

A Designer's inputs to VED (VLSI Education Day, India)

Abstract

This small article is aimed at introducing fresh VLSI graduates to some of the useful resources (books, web sites etc.). This list is neither exhaustive nor a "set of junk links" – these are the ones that we have used during our last two to two and half years of Industry experience. The main focus is on the front-end VLSI design (as this is my field of work, currently).

Introduction

Let me introduce myself as Srinivasan Venkataramanan (seenu_sridhar@yahoo.com, Venkataramanan.Srinivasan@Philips.com), an M.Tech pass-out from IITD (1996-97) and working with Philips Semiconductors, Eindhoven, Netherlands since 1998. I wish to share a few thoughts that I hope would be of some use to the fresh graduates in this VLSI area. My area of work is "**Front End ASIC Design**" which involves:

- Design from Specification
- Coding at RT Level (VHDL and/or Verilog)
- Synthesis (RTL to Gate Level netlist)
- IP (Intellectual Property) integration – to integrate blocks (like a micro-controller, video processor, USB etc.) to create a System On Chip (SoC) – given the specifications of the system and the blocks themselves.
- System Level Verification – creating Testbenches/ test cases to test a system (could be an SoC), given the specifications of the system and a model (could be RTL or Gate level)
- Simulation Methodologies – explore new simulation methodologies/alternatives and try and customize them to fit in Industry specific design flow. (e.g. Compiled-code simulation Vs Interpretive simulation, Cycle based simulation Vs Event-driven simulation).

Resources

HDLs – VHDL, Verilog

VHDL

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1.> **Vhdl for Programmable Logic**, by **Kevin Skahill** – a good book for Beginners, though the name suggests it is for "programmable logic" I found it EXTREMELY useful to start learning VHDL and best of all it is available for an affordable price in India.

Kevin Skahill, Jay Legenhausen, Ron Wade, Corey Wilner, BL Wilson
ISBN 0201895730, Addison-Wesley
May 1996, 593 pages, book & CD-Rom edition includes Cypress WARP
software and examples,
<http://www.amazon.com/exec/obidos/ISBN%3D0201895730/002-9583653-7021215>

2.> **VHDL Coding Styles and Methodologies, 2nd Edition - Ben Cohen** –
This is recommended for someone who knows “what is VHDL” and its basic semantics and would like to project himself/herself to a more decent and a methodologically good VHDL coding person. BEST industry oriented book I have seen till today.

ISBN 0-7923-8474-1, [Kluwer Academic Publishers](#)
1999, 450 pages. Book emphasizes detailed application of the language, style, methodologies, and synthesis through several complete examples. This edition provides practical information on reusable software methodologies for the design of bus functional models for testbenches. This includes the waveform, client/server, command text and binary file methods. All VHDL code is on CD. CD also includes the GNU toolsuite with EMACS language sensitive editor, TSHHELL, 30 day evaluation of ModelSim (Model Technology), and 20 day evaluation of Synplify (Synplicity). For TOC see <http://members.aol.com/vhdlcohen/vhdl>

Verilog

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1.> **Verilog Quickstart – by James M. Lee** – A simple (not very detailed though), real “quick start” book.

Kluwer Academic Publishers

ISBN: 0-7923-8515-2

The second edition of Verilog Quickstart includes some of the IEEE proposed changes to the Verilog IEEE1364-1999 standard.

The second edition also makes learning Verilog easier by the inclusion of a CDROM with the [SilosIII](#) Verilog simulator.

2.> **[The Verilog Hardware Description Language](#) by Donald E. Thomas, Philip R. Moorby** - Referred to as a VERY GOOD book by designers in the News Groups.

A valuable resource for engineers and students interested in describing, simulating and synthesizing digital systems.

3.> **[Verilog Hdl : A Guide to Digital Design and Synthesis](#) by Samir Palnitkar** – A very detailed book, BEST IMHO (in My Humble Opinion)

From the publisher: "This complete Verilog HDL reference progresses from the basic Verilog concepts to the most advanced concepts in digital design.

For more listings please visit

VHDL

<http://www.vhdl.org/comp.lang.vhdl/FAQ2.html>

Verilog

<http://www.verilog.net/books.html>

In general whenever you get a doubt on either of these HDLs do the following:

- 1.> Take a break and think ☺
- 2.> For VHDL there is an exhaustive FAQ located at:
<http://www.vhdl.org/comp.lang.vhdl/>
- 3.> For verilog, see <http://www.verilog.net/docs.html>
- 4.> The News Groups (a forum where people discuss about the language/its usage etc.) are THE BEST way to “uplift” a frsh graduate to an “industry oriented designer”. You can access them in several ways:
 - a.> Through a “NEWS SERVER” – if available.
 - b.> Via WEB – visit <http://www.deja.com> or <http://www.remarq.com> and register for FREE and subscribe yourself for the NGs of your choice. The ones that I use often are:

- comp.lang.vhdl
- comp.lang.verilog
- comp.cad.synthesis
- comp.cad.fpga

For Verilog-VHDL know-how (interoperatibility etc.) see:
<http://www.simucad.com/ArticleReprints/VRLG95A.html>

For more web sites, please see the appendix-A.

DSP related Publications

<http://www.kom.auc.dk/DSP/>

Mailing Lists

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Hemant Kumar, an M.Tech pass-out from IITD (1996-97) maintains a couple of “mailing lists” (via <http://www.egroups.com>) through which our colleagues share quite a lot of information. Perhaps you could request him to let you view the postings.

CAD Tools

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There are quite a number of tools which can help you to understand the design process better. There are a few HDL parsers for FREE and some are low-priced limited versions. They could be of great use to the universities having limited resource fundings. Also there are a few FREE EDA tools project. Please find a few of them listed below.

<http://www.flex.com/~jching> - a FREE Verilog Behavioural Simulator (VBS)

Also visit <http://www.verilog.net/free.html>

For VHDL tools, visit <http://www.vhdl.org/comp.lang.vhdl/FAQ3.html>

Appendix-A

A comprehensive list of Web sites are presented here alongwith a brief description.

Verilog Related Sites

- Verilog FAQ <http://www.angelfire.com/in/verilogfaq/index.html>
(<http://www.angelfire.com/in/verilogfaq/index.html>)
- An online Verilog Manual - Bucknell Handbook on Verilog HDL [Bucknell Verilog Manual](http://www.europa.com/~celiac/verilog-manual.html)
(<http://www.europa.com/~celiac/verilog-manual.html>)
-- This site contains general information about Verilog, synthesis using Synopsys and a little bit of information about VHDL
- [Celia's Verilog & EDA Web Page](http://www.europa.com/~celiac/ver_eda.html)
(http://www.europa.com/~celiac/ver_eda.html)
- EMACS Mode for Verilog [EMACS for Verilog](http://www.surefirev.com/emacs_install.html)
(http://www.surefirev.com/emacs_install.html)
- JAVA 2 Verilog – a Commercial startup firm: [LEAP JAVA2 Verilog Sign-up](http://www.lavalogic.com/join.html)
(<http://www.lavalogic.com/join.html>)
- A Good Online tutorial for Verilog [Online Verilog Tutorial](http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/manual/index.html)
(<http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/manual/index.html>)
- Open Verilog International – a body which is involved in Verilog LRM. [OVI Home Page](http://www.ovi.org/) (<http://www.ovi.org/>)
- Verilog-AMS page (Analog & Mixed Signal extensions) [OVI- Verilog-AMS](http://www.eda.org/verilog-ams/)
(<http://www.eda.org/verilog-ams/>)
- Another Good FAQ for Verilog.. [Rajesh Bawankule's HomePage](http://www.angelfire.com/in/rajesh52/verilog.html)
(<http://www.angelfire.com/in/rajesh52/verilog.html>)
- A detailed, on-line Verilog Standard/Keyword browser. [SEVA The HDL Authority](http://www.intrinsix.com/Verilog_guide/index.htm) (http://www.intrinsix.com/Verilog_guide/index.htm)

- [Verilog Beginner's Guide](http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/index.html)
(<http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/index.html>)
- Interactive Verilog FAQ/hint page Hints Questions and Answers [Verilog FAQ](http://c118618-a.frmt1.sfba.home.com/faq/verilog) (<http://c118618-a.frmt1.sfba.home.com/faq/verilog>)
- Looking for an Exhaustive Verilog models (for an evaluation perhaps) [Verilog Files used for the ISD magazine benchmark](http://c118618-a.frmt1.sfba.home.com/isd/)
(<http://c118618-a.frmt1.sfba.home.com/isd/>)
- [VERILOG INTRODUCTION FOR DIGITAL DESIGN](http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/index.html)
(<http://www.ee.ed.ac.uk/~gerard/Teach/Verilog/index.html>)
- [Verilog-2000 Information Page by Sutherland HDL, Inc.](http://www.verilog-2000.com/) – Contains the significant changes being proposed in the Verilog-2000 Standard.
(<http://www.verilog-2000.com/>)
- [Verilog.Net - Premiere List of Verilog Resources on the Internet](http://www.verilog.net/)
(<http://www.verilog.net/>)
- [VPP - Verilog Pre Processor](http://www.surefirev.com/vpp/vpp.html) – A preprocessor for Verilog files (typically used in industries)
(<http://www.surefirev.com/vpp/vpp.html>)
- [Welcome to Project VeriPage](http://www.angelfire.com/ca/verilog/) – Contains whole lot of information on Verilog, Pli etc. (PLI – Programmable Language Interface to Verilog, through which you can interact with the Verilog design using C)
(<http://www.angelfire.com/ca/verilog/>)

VHDL Related Sites

- [FAQ comp.lang.vhdl - THE Source for VHDL!! - Kept up-to-date](http://vhdl.org/comp.lang.vhdl/)
(<http://vhdl.org/comp.lang.vhdl/>)
- [An Introduction to VHDL](http://www.acc-eda.com/h_intro.htm) - A simple introduction into VHDL and its Usage
(http://www.acc-eda.com/h_intro.htm)
- [Analysis of Parallel VHDL Simulation](http://einstein.et.tudelft.nl/~heco/chess/p/p.html) - A Project undertaken at Tech. Univ. Eindhoven.
(<http://einstein.et.tudelft.nl/~heco/chess/p/p.html>)
- [CPLD, FPGA The Programmable Logic Jump Station](http://www.optimagic.com/index.shtml) - Good info on CPLD, FPGA etc.
(<http://www.optimagic.com/index.shtml>)
- [Digital System Design with VHDL](#) - by Mark Zwolinski

(<http://www.ecs.soton.ac.uk/~mz/VHDL/>)

- [ESTEC External Home Page](#) - EUROPEAN SPACE RESEARCH AND TECHNOLOGY CENTRE
(<http://www.estec.esa.nl/>) - Contains some good coding guidelines besides other stuff.
- [External VHDL Links](#) - A good set of Links to VHDL sites
(http://www.cscs.wmin.ac.uk/~seamang/VHDL/vhdl_links.html)
- [FMF Home Page](#) - Free Model Foundation - has lot of free models!!
(<http://www.vhdl.org/fmf/>)
- [FPGA Synthesis at Duke](#)
(http://www.ee.duke.edu/Research/VHDL_tutorial/)
- [FPGA VHDLfrom APS](#)
(<http://www.associatedpro.com/aps/x84lab/>)
- [Getting started with programmable logic](#)
(<http://www.geocities.com/SiliconValley/Code/1835/starter.html>)
- [GMD FOKUS - Error Correction Code site](#) - Good info on Programmable Logic
(<http://www.fokus.gmd.de/research/cc/mobra/products/fec/content.html>)
- [Green Mountain VHDL Tutorial](#)
(<http://www.gmvhdl.com/VHDL.html>)
- <http://rassp.scra.org/vhdl/index.html> - RASSP Support Page for VHDL
(<http://rassp.scra.org/>)
- [IEEE 1076.1](#) - An initiative to develop and to maintain analog and mixed-signal extensions to the VHDL language (<http://www.vhdl.org/vi/analog/>)
- [IEEE Standards Products Catalog - Design Automation](#) - Where to Buy the LRMs?? (<http://standards.ieee.org/catalog/design.html>)
- [LEON-1 SPARC VHDL model](#) - A VHDL Model for SPARC
(<http://www.estec.esa.nl/wsmwww/leon/>)
- [LFSR testbench](#) - A Good (FREE!) simple tool to create VHDL/Verilog for LFSR
(<http://www.jps.net/kyunghi/LFSR/>)
- [Links to HDL WWW Servers](#)
(<http://www.mrc.uidaho.edu/cgi-bin/w3-mysql/vlsi/CADHDL.html>)
- [List of free VHDL models and packages !](#)
(http://erm1.u-strasbg.fr/db/mod_db_out.phtml)
- [Microprocessor Soft Cores from VAutomation Inc.](#)
(<http://www.80186.com/>)
- [Model Hotlist](#)
(http://vhdl.org/fmf/wwwpages/model_hotlist.html)

- [Northeastern University VHDL Design & Development](http://www.ece.neu.edu/info/vhdl/vhdl.html)
(http://www.ece.neu.edu/info/vhdl/vhdl.html)
- [Papers from VIUF](http://www.vhdl.org/viuf/papers/)
(http://www.vhdl.org/viuf/papers/)
- [SEAMS Homepage ...](http://www.ececs.uc.edu/~mistie/)
(http://www.ececs.uc.edu/~mistie/)
- [SPICE To VHDL-AMS Translator](http://www.ececs.uc.edu/~rmayilad/translator.html)
(http://www.ececs.uc.edu/~rmayilad/translator.html)
- [The Free IP Project](http://www.free-ip.com/)
(http://www.free-ip.com/)
- [VHDL & Cycle Based Simulation](http://www.vhdl.org/vhdl_intl/vltimes/52-MURALI.html)
(http://www.vhdl.org/vhdl_intl/vltimes/52-MURALI.html)
- [VHDL International Users Forum \(VIUF\)](http://www.vhdl.org/viuf/)
(http://www.vhdl.org/viuf/)
- [VHDL Introduction](http://www.ece.uc.edu/~rmiller/VHDL/intro.html)
(http://www.ece.uc.edu/~rmiller/VHDL/intro.html)
- [VHDL Synthesis Guide](http://eepad.sogang.ac.kr/~chang/vhdl/)
(http://eepad.sogang.ac.kr/~chang/vhdl/)
- [VHDL Synthesis Interoperability Working Group](http://www.vhdl.org/vhdlsynth/siwg/)
(http://www.vhdl.org/vhdlsynth/siwg/)
- [VHDL SYNTHESIS TUTORIAL - BOB REESE - JUNE 1995](http://www.erc.msstate.edu/~reese/vhdl_synthesis/)
(http://www.erc.msstate.edu/~reese/vhdl_synthesis/)
- [VHDL Tutorial from Germany](http://www.vhdl-online.de/~vhdl/TUTORIAL/)
(http://www.vhdl-online.de/~vhdl/TUTORIAL/)
- [VHDL Verification Course](http://www.i2.i-2000.com/~stefan/vcourse/html/file_read.html)
(http://www.i2.i-2000.com/~stefan/vcourse/html/file_read.html)
- [VHDL-AMS RELATED SITES](http://esaki.ee.boun.edu.tr/~cosgul/vhdl_ams/index.htm)
(http://esaki.ee.boun.edu.tr/~cosgul/vhdl_ams/index.htm)
- [VHDL-AMS Scanner on the internet!](http://www.syssim.ecs.soton.ac.uk/vhdl-ams/web-parser/web-parser.html)
(http://www.syssim.ecs.soton.ac.uk/vhdl-ams/web-parser/web-parser.html)
- [VHDL-GUI](http://www.atl.external.lmco.com/rassp/vgui/index.html)
(http://www.atl.external.lmco.com/rassp/vgui/index.html)
- [VHDLSynth \(1076.3\) Home page](http://www.vhdl.org/vhdlsynth/)
(http://www.vhdl.org/vhdlsynth/)
- [WAVES - IEEE Std 1029.1-1991 - Description](http://standards.ieee.org/reading/ieee/std_public/description/dasc/1029.1-1991_desc.html)
(http://standards.ieee.org/reading/ieee/std_public/description/dasc/1029.1-1991_desc.html)

- [WAVES Home Page](http://vhdl.org/vi/waves/)
(http://vhdl.org/vi/waves/)
- <http://icosym.cvut.cz/cacsd/msa/>
(http://icosym.cvut.cz/cacsd/msa/)
- [CACSD MSA Index](http://icosym.cvut.cz/cacsd/msa/)
(http://icosym.cvut.cz/cacsd/msa/) General Technical Sites

ASIC Related Sites

- [80C51 HomePage for Lance Dannan Bresee](http://www.ucolick.org/~lance/home.html)
(http://www.ucolick.org/~lance/home.html)
- [App Note Abstract FIFO ARCHITECTURE, FUNCTIONS, AND APPLICATIONS](http://www.ti.com/sc/docs/psheets/abstract/apps/scaa042a.htm)
(http://www.ti.com/sc/docs/psheets/abstract/apps/scaa042a.htm)
- [ASICs... the website](http://www.dacafe.com/Book/)
(http://www.dacafe.com/Book/)
- [Downloads 80C51](http://www.dunfield.com/download.htm)
(http://www.dunfield.com/download.htm)
- [Getting Started With Programmable Logic](http://www.geocities.com/SiliconValley/Code/1835/starter.html)
(http://www.geocities.com/SiliconValley/Code/1835/starter.html)
- [Integrated System Design Magazine - isdmag.com](http://www.isdmag.com/)
(http://www.isdmag.com/)
- [Intel Pentium Pro Processor Presentation \(Index\)](http://pentium.intel.com/procs/p6/isscc/index.htm)
(http://pentium.intel.com/procs/p6/isscc/index.htm)
- [Lance Dannan Bresee's 8051 Code Page](http://www.ucolick.org/~lance/8051/8051.html)
(http://www.ucolick.org/~lance/8051/8051.html)
- [Motorola Semiconductor Reuse Standards](http://www.mot-sps.com/technology/srs/)
(http://www.mot-sps.com/technology/srs/)

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- [DV & Firewire Central What is DV \(DVCAM, DVCPRO\)](http://www.dvcentral.org/dvwhat.html)
(http://www.dvcentral.org/dvwhat.html)
- [FireWire Devices Spark For Mac Users](http://www.techweb.com/wire/story/TWB19990722S0013)
(http://www.techweb.com/wire/story/TWB19990722S0013)
- [Philips Semiconductors; IEEE1394 Multimedia Bus](http://www.semiconductors.philips.com/1394/)
(http://www.semiconductors.philips.com/1394/)
- [Remote User Available Mailing Lists](http://mail.dvcentral.org/guest/RemoteListSummary/1394)
(http://mail.dvcentral.org/guest/RemoteListSummary/1394)

Free EDA

- [Alliance Home Page - FREE EDA Tools, VHDL Compiler](http://www-asim.lip6.fr/alliance/)
(http://www-asim.lip6.fr/alliance/)
- [Beige Bag Software \\$299 !!](http://www.beigebag.com/)
(http://www.beigebag.com/)
- [Beige Bag Software Educational Pricing](http://www.beigebag.com/pricing_univ.htm)
(http://www.beigebag.com/pricing_univ.htm)
- [CAD FARM www.cadfarm.com](http://www.cadfarm.com/)
(http://www.cadfarm.com/)
- [DACafe EDA Downloads EDA Utilities](http://www.dacafe.com/DACafe/links/pages/EDA_Uilities/)
(http://www.dacafe.com/DACafe/links/pages/EDA_Uilities/)
- [FREE LINUX BASED TOOLS -public-ftp-pub-Linux-apps-circuits](ftp://sunsite.unc.edu/pub/Linux/apps/circuits/!INDEX.html)
(ftp://sunsite.unc.edu/pub/Linux/apps/circuits/!INDEX.html)
- [Freeware EDA Tools Page](http://www.v-ms.com/)
(http://www.v-ms.com/)
- [GNU gEDA Tools - Programs](http://www.geda.seul.org/tools/index.html)
(http://www.geda.seul.org/tools/index.html)
- [Spice Resource](http://www.cadfarm.com/spice.htm)
(http://www.cadfarm.com/spice.htm)
- [SPICE Tools FREE http--www.ece.ucdavis.edu-sscr-clcfaq-faq-faq-toc.html](http://www.ece.ucdavis.edu/sscr/clcfaq/faq/faq-toc.html)
(http://www.ece.ucdavis.edu/sscr/clcfaq/faq/faq-toc.html#TOC)
- [Whiteley Research Incorporated](http://www.srware.com/)
(http://www.srware.com/)
- [WRC Pricing of tools http--www.srware.com-prices.html](http://www.srware.com/prices.html)
(http://www.srware.com/prices.html)
- [Linux EDA](http://www.linuxeda.com/)
(http://www.linuxeda.com/)

FSM Extraction

- [Cisco FSM Home Page](http://www.employees.org/~ciscofsm/)
(http://www.employees.org/~ciscofsm/)
- [Download Renoir Demos](http://www.mentor.com/renoir/download_form.htm)
(http://www.mentor.com/renoir/download_form.htm)
- [FSM Library](http://www.research.att.com/sw/tools/fsm/)
(http://www.research.att.com/sw/tools/fsm/)

- [graphviz](http://www.research.att.com/sw/tools/graphviz/)
(http://www.research.att.com/sw/tools/graphviz/)
- [Practical FSM Analysis for Verilog](http://www.employees.org/~ciscofsm/fsmSlides/)
(http://www.employees.org/~ciscofsm/fsmSlides/)
- [Products Overview](http://www.novassoft.com/products/products.htm) – NOVAS RTL Debugger!
(http://www.novassoft.com/products/products.htm)
- [Summit Design, Inc. Visual HDL](http://www.summit-design.com/products/visual.html)
(http://www.summit-design.com/products/visual.html)

TCL

- [Dan Wallach Hacks](http://www.cs.rice.edu/~dwallach/hacks.html)
(http://www.cs.rice.edu/~dwallach/hacks.html)
- [Tcl Tk Information](http://www.tcltk.com/)
(http://www.tcltk.com/)
- [The Tcl Platform Company - Scriptics](http://www.scriptics.com/)
(http://www.scriptics.com/)
- [The World-Wide Web Virtual Library Tcl and Tk](http://cuiwww.unige.ch/eao/www/TclTk.html)
(http://cuiwww.unige.ch/eao/www/TclTk.html)
- [Yahoo! Computers and Internet Programming Languages Tcl Tk](http://dir.yahoo.com/Computers_and_Internet/Programming_Languages/Tcl_Tk/)
(http://dir.yahoo.com/Computers_and_Internet/Programming_Languages/Tcl_Tk/)
- [Logic in Computer Science authors titles recent](http://xxx.lanl.gov/list/cs.LO/recent)
(http://xxx.lanl.gov/list/cs.LO/recent)
- [LookSmart - exploring - Computers & Internet - Computer Science - Programming - Internet & Scripting](http://www.looksmart.com/eus1/eus53832/eus155852/eus53906/eus65717/r?l&ieey&)
(http://www.looksmart.com/eus1/eus53832/eus155852/eus53906/eus65717/r?l&ieey&)
- [Matt's Script Archive](http://www.worldwidemart.com/scripts/)
(http://www.worldwidemart.com/scripts/)
- [Perl Documentation](http://language.perl.com/info/documentation.html)
(http://language.perl.com/info/documentation.html)
- [Ptolemy](http://ptolemy.eecs.berkeley.edu/) – H/W S/W Co-Design Environment, UCB
(http://ptolemy.eecs.berkeley.edu/)
- [LVDS line impedance calculator](http://www.jps.net/kyunghi/LVDS/)
(http://www.jps.net/kyunghi/LVDS/)

Tools, Vendors etc (Commercial)

- [- Cogency Technology -](http://www.cogency.com/tech/index.htm)
(http://www.cogency.com/tech/index.htm)
- [About Our Products](http://www.interhdl.com/products.html)
(http://www.interhdl.com/products.html)
- [Analogy - Leader in Mixed Signal Simulation](http://www.analogy.com/home.htm)
(http://www.analogy.com/home.htm)
- [Averant, Inc., The Leader in Static Functional Verification](http://www.averant.com/index.htm)
(http://www.averant.com/index.htm)
- [C Level Design](http://www.cleveldesign.com/)
(http://www.cleveldesign.com/)
- [Cheap P&R ICAD Homepage](http://www.internetcad.com/)
(http://www.internetcad.com/)
- [ChipCenter The Web's First Definitive Electronics Resource](http://www.chipcenter.com/)
(http://www.chipcenter.com/)
- [CyclopsPro Product Info](http://www.topdown.com/cyclopspro/index.htm)
(http://www.topdown.com/cyclopspro/index.htm)
- [CyclopsPro Gates Data Sheet](http://www.topdown.com/cyclops/datasht.htm)
(http://www.topdown.com/cyclops/datasht.htm)
- [CynApps PRODUCTS CynApps Suite](http://www.cynapps.com/CynApps/products/suite/index.html)
(http://www.cynapps.com/CynApps/products/suite/index.html)
- [DAC Online - Cadence](http://dac.cadence.com/)
(http://dac.cadence.com/)
- [Deep Chip Home Page](http://www.DeepChip.com/)
(http://www.DeepChip.com/)
- [Design Automation Cafe](http://www.dacafe.com/)
(http://www.dacafe.com/)
- [Easics' Web Tools](http://www.easics.com/wwwtools/wwwtools.html)
(http://www.easics.com/wwwtools/wwwtools.html)
- [EDA Books Online](http://www.dacafe.com/DACafe/EDATools/EDAbooks/EDAbooks.html)
(http://www.dacafe.com/DACafe/EDATools/EDAbooks/EDAbooks.html)
- [EDTN Home](http://www.edtn.com/)
(http://www.edtn.com/)
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